Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices

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This letter describes the fabrication and structural and electrical characterization of an aerosol-nanocrystal-based floating-gate field-effect-transistor nonvolatile memory. Aerosol nanocrystal nonvolatile memory devices demonstrate program/erase characteristics comparable to conventional stacked-gate nonvolatile memory devices. Aerosol nanocrystal devices with 0.2 μm channel lengths exhibit large threshold voltage shifts (>3 V), submicrosecond program times, millisecond erase times, excellent endurance ($>10^5$ program/erase cycles), and long-term nonvolatility ($>10^6$ s) despite thin tunnel oxides (55–60 Å). In addition, a simple aerosol fabrication and deposition process makes the aerosol nanocrystal memory device an attractive candidate for low-cost nonvolatile memory applications. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1385190]

We have fabricated floating-gate metal–oxide–semiconductor field-effect transistors (MOSFETs) in which the conventional stacked gate has been replaced with silicon nanocrystals formed and deposited as an aerosol. The memory operation of the aerosol nanocrystal floating-gate MOSFET depends on charge storage in the floating-gate, similar to conventional stacked-gate nonvolatile memory devices.[1] In a silicon nanocrystal nonvolatile memory device, however, charge is not stored on a continuous floating-gate polysilicon layer as is the case in conventional stacked-gate devices, but on a discontinuous floating-gate layer composed of discrete crystalline silicon nanocrystals.[2–4] Nanocrystal charge storage offers several potential advantages over conventional stacked-gate nonvolatile memory devices; (1) a simple low cost floating-gate fabrication process; (2) improved retention resulting from Coulomb blockade and quantum confinement effects[5] that enable the use of thinner tunnel oxides and lower operating voltages; (3) reduced punch-through achieved by eliminating drain-to-floating-gate coupling, allowing higher drain voltages during readout, shorter channel lengths, and smaller cell area; and (4) excellent immunity to stress induced leakage current and defects within the floating-gate or insulating layers due to the distributed nature of the charge storage in the discontinuous nanocrystal layer.

The potential for improved device performance and reliability strongly depends upon the ability to control particle core size, particle size distribution, crystallinity, areal particle density, oxide-passivation quality, and crystal-to-crystal insulation that prevents lateral charge conduction in the nanocrystal layer. In order to achieve the desired layer properties, we have developed a three-step nanocrystal fabrication process. Details of silicon nanocrystal synthesis and deposition onto 200 mm wafers can be found in a separate reference.[6] A continuous flow reactor generates silicon nanocrystal aerosol by silane pyrolysis at 950 °C. Nanocrystals form by homogeneous nucleation and grow by chemical vapor deposition. Through the hot zone of the reactor, they are sintered to form dense spherical single crystal nanocrystals. Silane concentration, furnace temperature, and residence time have been optimized to generate an aerosol of nonagglomerated spherical single crystal nanocrystals with diameters as small as 3 nm.

In the second reactor, a 1–2 nm high-quality thermal oxide shell is grown at 1050–1100 °C on the nanocrystals. This insulating oxide shell reduces lateral crystal-to-crystal conduction in the nanocrystal layer even when nanocrystals are deposited at sufficient densities to be in contact with each other on the wafer. The thermal oxide also prevents the formation of a lower quality room temperature native oxide on the nanocrystals once they are exposed to ambient cleanroom environments.

In these nanocrystal memory devices, two different aerosol nanocrystal samples are produced: (i) average crystalline core diameter of 4 nm, $\sigma_g = 1.3$ with 1.5 nm SiO_2 passivating layer and (ii) average crystalline core diameter of 8 nm, $\sigma_g = 1.4$ with 2.0 nm SiO_2 passivating layer. A monolayer of these oxide-passivated nanocrystals is integrated into 0.2 μm

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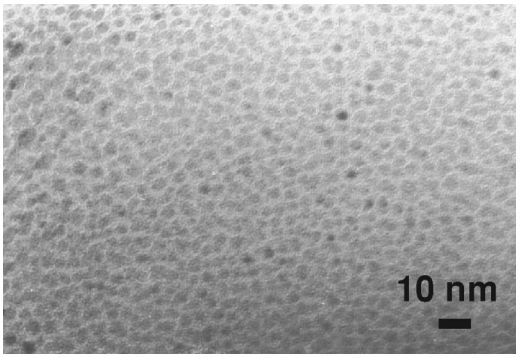

FIG. 1. Plan view transmission electron microscopy of an aerosol silicon nanocrystal floating-gate. The average nanocrystal diameter is 4 nm and $\sigma_g = 1.3$ with density 6×10^{12} nanocrystals cm^{-2}.

*n*MOS transistors by thermophoretic deposition of the aerosol nanocrystals onto 200 mm silicon wafers with 4, 5, or 7 nm thermally grown tunnel oxide. The deposited nanocrystal layer can approach densities as high as 10^{13} nanocrystals cm^{-2} for 4 nm diameter nanocrystals. Device fabrication continues by covering the nanocrystal layer with either 8 or 12 nm chemical vapor deposited high temperature oxide to embed the nanocrystal floating-gate in oxide prior to polysilicon gate deposition.

The aerosol technique has resulted in nanocrystal layers with narrow size distributions, high-quality oxide passivation, and good areal coverage, as illustrated by plan view transmission electron microscopy in Fig. 1. High-resolution cross-sectional transmission electron microscopy (not shown) confirms that average diameter 4 nm crystalline nanocrystals are incorporated in the gate dielectric stack. The measured tunnel oxide thickness of 5.5 nm represents the sum of the wafer thermal oxide (4 nm) and the nanocrystal oxide shell (1.5 nm).

Most of the electrical characterization results (e.g., program, erase, turn on, retention, and endurance) were similar for the floating-gate comprised of the 4 nm silicon core nanocrystals and the 8 nm silicon core nanocrystals. However, the gate disturb data for the 4 nm nanocrystal floating-gate indicated floating to control gate leakage. The electrical measurements presented in this letter were taken from the same 0.2 μm channel length device composed of 8 nm silicon core, 2 nm SiO_2 shell nanocrystal floating-gate, 5 nm tunnel oxide, and 8 nm high temperature oxide.

Subthreshold characteristics of the 0.2 μm channel length aerosol-nanocrystal MOSFET are shown in Fig. 2(a), and output characteristics are shown in Fig. 2(b). The values of the drive current (30 μA/μm), the subthreshold slope (200 mV/dec), and the drain induced barrier lowering (100 mV/V) are typical for thick gate dielectric, high substrate doped nonvolatile memory devices. The threshold voltage V_t is defined as the gate voltage corresponding to a 1 μA drain–source current when a 1 V drain bias is applied.

Uniform Fowler–Nordheim tunneling is used to program and erase the memory, although programming with channel hot-electron injection is also possible. As shown in Figs. 3(a) and 3(b), the high areal nanocrystal density obtained by the aerosol fabrication process results in a large threshold voltage window (>3 V), larger than those previously reported on nanocrystal devices.[4,7] This large V_t win-

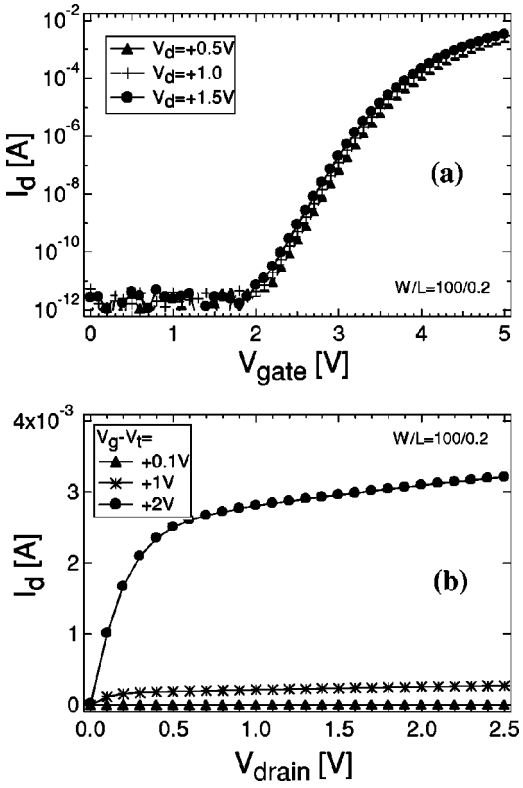

FIG. 2. (a) Subthreshold and (b) output characteristics of a 0.2 μm channel length aerosol nanocrystal floating-gate MOSFET. Subthreshold slope $= 200$ mV/dec; drive current $= 30$ μA/μm; drain induced barrier lowering $= 100$ mV/V.

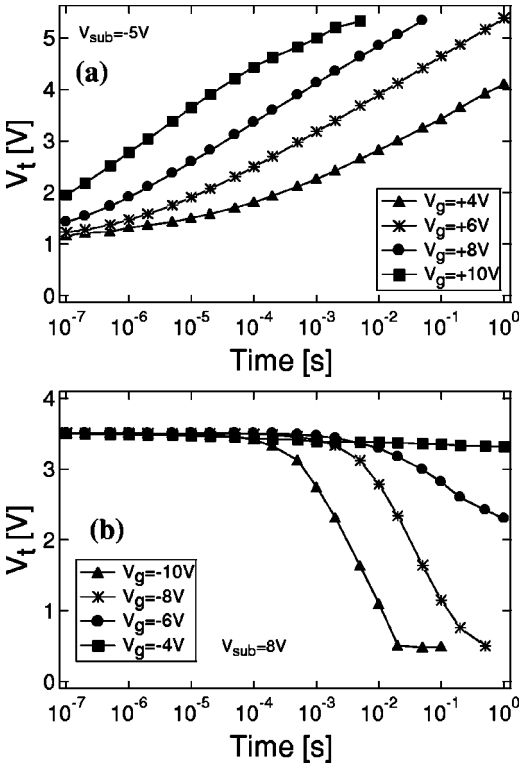

FIG. 3. (a) Program transients of a 0.2 μm channel length aerosol nanocrystal floating-gate MOSFET. The device programs to $V_t = 3.3$ V in 50 μs with gate and substrate bias of $+8$ and -5 V, respectively. (b) Erase transients of the same 0.2 μm channel length aerosol nanocrystal floating-gate MOSFET. The device erases to $V_t = 1$ V in 100 ms with gate and substrate bias of -7 and 8 V, respectively.

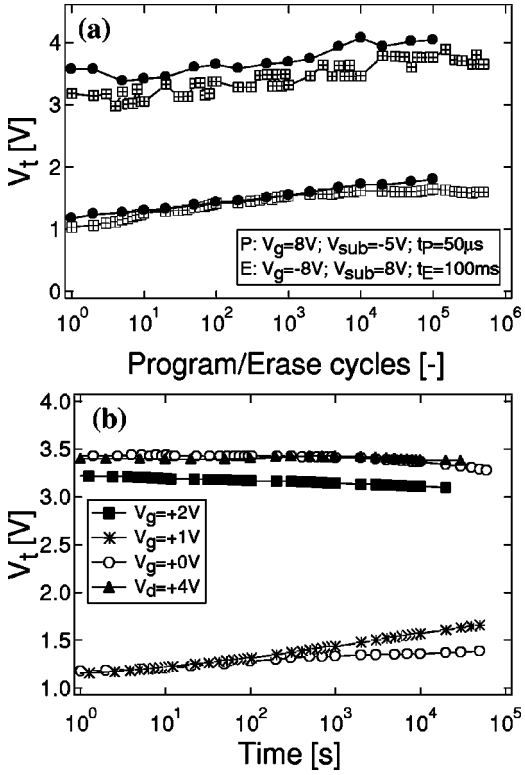

FIG. 4. (a) Endurance characteristics of a 0.2 μm channel length aerosol nanocrystal floating-gate MOSFET. Only limited window closure is observed after 10^5 program/erase cycles. (b) Disturb characteristics of a 0.2 μm channel length aerosol nanocrystal floating-gate MOSFET after 10^5 program/erase cycles. Unless otherwise indicated, all nodes are grounded.

dow results in a high read-out current (20 μA/μm for gate and drain biases of 2.5 and 1 V, respectively), allowing fast memory access. The transient characteristics illustrate the voltage/performance tradeoff for this device; higher voltages result in faster program and erase times. Despite the low gate coupling ratio inherent to nanocrystal memories, microsecond programming and millisecond erasure are possible at moderate operating voltages.

We have also measured erase transients with the same bias conditions after programming the device to threshold voltages ranging from $V_t = 1.8$ V to $V_t = 3.5$ V. From a comparison of the erase transients (not shown), the rate of change in V_t only depends upon the current value of V_t and is independent of the program/erase history that lead to that V_t. This observation is consistent with the Fowler–Nordheim tunneling mechanism and indicates that charge is stored in traps/nanocrystals with a well-defined distance from the channel and a well-defined energy with respect to the silicon conduction band. This behavior is not expected for charge trapping centers that are randomly distributed throughout the gate oxide and/or have energy levels with a wide distribution in energy.

As shown in Fig. 4(a), the aerosol devices demonstrate excellent endurance behavior with only a small window closure observed after 5×10^5 cycles. Both the program and erase values shift slightly during cycling due to filling of fixed charge states. This gradual shift of the V_t window to higher threshold voltages indicates charge buildup in the gate-oxide layer during cycling. This charge buildup is reversible and can be removed by imposing higher erase voltages across the device.

Disturb and retention data after program/erase cycling is presented in Fig. 4(b). In spite of the thin tunnel oxide, reasonable disturb times, and long nonvolatility are obtained, indicative of the intrinsic advantage of discrete nanocrystal charge storage. However, further gate dielectric stack optimization is necessary to claim true nonvolatile behavior. No stress-induced leakage current was observed. Also, no drain disturb was detected, even at drain voltages as high as 4 V. This observation indicates that there is little or no lateral conduction in the nanocrystal layer.

An aerosol-based technique has been used to integrate a very dense ($\sim10^{13}$ nanocrystals cm^{-2}), coplanar, and uniform layer of nonagglomerated, spherical, single crystal nanocrystals in the gate dielectric of 0.2 μm channel length MOSFET devices. As a result of the distributed charge storage in the floating-gate layer, the aerosol nanocrystal MOSFET devices possess very good electrical nonvolatile characteristics, including a high read-out current, promising disturb behavior, excellent endurance, absence of stress-induced leakage current, and long-term charge retention after cycling.

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[1] S. Lai, Y. W. Hu, S. Tam, G. K. Lum, and V. K. Dham, Tech. Dig. Int. Electron Devices Meet., 468 (1984).
[2] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chen, and D. Buchanan, Tech. Dig. Int. Electron Devices Meet., 521 (1995).
[3] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE Trans. Electron Devices **41**, 1628 (1994).
[4] H. I. Hanafi, S. Tiwari, and I. Khan, IEEE Trans. Electron Devices **43**, 1553 (1996).
[5] S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, Appl. Phys. Lett. **69**, 1232 (1996).
[6] M. L. Ostraat, J. W. De Blauwe, M. L. Green, L. D. Bell, H. A. Atwater, and R. C. Flagan, J. Electrochem. Soc. **148**, G265 (2001).
[7] K. Saito, Y. Shi, H. Ishikuro, and T. Hiramoto, IEEE Silicon Nanoelectronics Workshop, 1998, P. 17.